i) hardware on the decoder for adjusting the local clock frequency until a threshold condition occurs, and

ii) a processor on the decoder and having a software program for adjusting the local clock frequency after the threshold condition occurs.

REMARKS

Claims 1-5, 7-10 and 13-15 are pending in this application. In the Office Action, the Examiner allowed Claims 1 and 7-10, and Claims 2-5 and 13-15 were rejected under 35 U.S.C. 112 as being indefinite. None of Claims 2-5 and 13-15 were rejected over the prior art, and the Examiner indicated that these claims would be allowable if rewritten to overcome the rejections under 35 U.S. 112.

Applicant is herein amending Claims 2, 3 and 13 to overcome the rejections of Claims 2-5 and 13-15.

More specifically, Claim 2 is being amended to establish a better correspondence between claim 1 and Claim 2. In particular, material now included in Claim 1 is being deleted from the preamble and the body of Claim 2, and lines 9-12 of Claim 2 (as presented herein) are being rephrased to more clearly distinguish between the received program clock signals and the program clock value maintained at the decoder. It is respectfully submitted that the changes made herein to Claim 2 overcome the indefiniteness of the claim.

Claim 3, lines 8-10, is also being amended to better distinguish between the received program clock signals and the program clock value maintained at the decoder. These amendments to Claim 3 overcome the indefiniteness of the Claim of Claims 4 and 5, which are dependent from Claim 3.

Claim 13 is being amended to positively set forth "a local clock value" and "a program clock value," to change "value" to "frequencies" in line 7, and to change "program value" to "program clock value" in line 8. These changes to Claim 13 overcome the indefiniteness of claim 13 and of Claims 14 and 15, which are dependent from Claim 13.

As amended herein, all of Claims 2-5 and 13-15 are clear and definite and fully comply with the requirements of 35 U.S.C. 112. The Examiner is, accordingly, respectfully requested to reconsider and to withdraw the rejections of these claims under 35 U.S.C. 112.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned "Version with markings to show changes made."

Every effort has been made to place this case in condition for allowance, a notice of which is requested. If the Examiner believes that a telephone conference would be advantageous to the disposition of this case, the Examiner is requested to telephone the undersigned.

Respectfully submitted,

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Serial No.: 09/052,673 Docket: END919980042US1 (11232)

"VERISON WITH MARKINGS TO SHOW CHANGES MADE"

IN THE CLAIMS:

Claims 2, 3 and 13 have been amended as follows:

--2. (Once Amend) A method according to Claim 1, [for adjusting a local clock of a digital data decoder,] wherein the local clock oscillates at [a] the local clock frequency, the method further comprising the steps of:

maintaining a local clock value based on the oscillations of the local clock;

receiving clock time stamps at the decoder which specify the program clock [value] signals and the frequency of the program clock;

maintaining a program clock value based on the program clock signals received at the decoder;

[determining if there is any difference between the local clock and the program clock frequencies;]

determining if there is an absolute difference between the local clock value and the program clock value;

if there is [either a difference between the local clock and the program clock frequencies or] an absolute difference between the local clock value and the program clock value, then adjusting the frequency at which the local clock oscillates so that said difference approaches zero.

3. (Thrice Amended) A method of synchronizing the frequency of a local clock of a digital data decoder with the frequency of a program clock, wherein the local clock oscillates at a local clock frequency, the method comprising the steps of:

determining the difference between the local and program clock frequencies, then adjusting the frequency at which the local clock oscillates so that said difference approaches zero;

maintaining a local clock value based on the oscillations of the local clock;

receiving clock time stamps at the decoder which specify [the] program clock [value] signals and the program clock frequency;

maintaining a program clock value based on the program clock signals received at the decoder;

determining if there is any difference between the local clock frequency and the program clock [frequencies] frequency;

determining if there is an absolute difference between the local clock value and the program clock value;

if there is either a difference between the local clock frequency and the program clock [frequencies] frequency or an absolute difference between the local clock value and the program clock value, then adjusting the frequency at which the local clock oscillates so that said difference approaches zero;

wherein the decoder includes hardware for adjusting the local clock frequency and a processor having a software program for adjusting the local clock frequency, and wherein the step of adjusting the frequency of the local clock includes the steps of:

using the hardware to adjust the local clock frequency until a threshold condition occurs; and

after the threshold condition occurs, using the processor to adjust the local clock frequency.

13. (Twice Amended) A system for synchronizing the frequency of a local clock of a digital data decoder with the frequency of a program clock, comprising:

means for determining if there is any difference between the local and program clock frequencies;

means for determining if there is an absolute difference between the local clock value and the program clock value; and

means for adjusting the frequency at which the local clock oscillates, when there is a difference between the local clock and the program clock [values] frequencies, or an absolute difference between the local clock value and the program clock value, so that said difference approaches zero, wherein the means for adjusting includes

i) hardware on the decoder for adjusting the local clock frequency until a threshold condition occurs, and

ii) a processor on the decoder and having a software program for adjusting the local clock frequency after the threshold condition occurs.